Bias circuit for High Yield Self-bias MMIC Amplifier for APAAs

Koji Yamanaka, Kazutomi Mori, Hiroshi Ikematsu, Yoshinobu Sasaki and Masatoshi Nakayama

Mitsubishi Electric Corporation

Abstract — **In this paper, a Ka-band self-bias Low-Noise MMIC amplifier is presented, which is equipped with a bias circuit that compensates gain variation of self-bias amplifier between chips due to process variations. The Ka-band low noise MMIC amplifier with proposed bias circuit was designed and manufactured. It was proved that the proposed bias circuit reduced the gain variation between chips from 0.8 dB RMS to 0.3 dB RMS. This amplifier is suitable for active phased array applications.**

I. INTRODUCTION

Recently, some active phased array antenna (APAA) systems are proposed for commercial communication systems, e.g. LEO satellite communication systems [1]-[2], and an airplane antenna system [3]-[5]. For commercial success, cost reduction is essential and cost of MMICs, which sometimes dominates the cost of Tx/Rx modules, should be reduced. Many works have been dedicated to realize miniature MMIC amplifiers for low cost [5]-[7].

In addition to the efforts to minimize chip size of the MMICs, to make Tx/Rx module cost more reasonable, it is very important to eliminate any costs accompanying with MMIC amplifiers, such as negative voltage generators for gate bias of FETs or external bias tuning circuits. Especially, for use in active phased array antennas, MMIC amplifiers are requested to show small variations between chips to achieve stringent tracking requirements without expensive additional constant current circuits.

Self-bias circuit is often used to realize single bias operation of FET amplifiers and to suppress the effect of process variations [5,6]. The feedback resistor of self-bias circuit not only eliminates need for negative bias but also works as like a constant current circuit by itself. However, to reduce the gain variation of self-bias amplifiers well enough for APAA application, the value of the feedback resistor should be so high that the dissipated power at the feed back resistor becomes not so negligible.

Another way to reduce the gain variation due to process variations is to set the operation bias point so that transconductance of FET shows its maximum. This way tends to increase the power dissipations more than required. Moreover, it may sacrifice the noise performance of low-noise amplifiers, for smallest Fmin usually appears at lower drain current than transconductance maximum.

In the last IMS conference, the authors have demonstrated simultaneous temperature and process variation compensation bias circuit for non self-bias low noise MMIC amplifier [8], in which another FET in addition to diodes for temperature compensation of amplifiers [9] has been employed. In this paper we have expanded that work for the case of self-bias MMIC amplifiers. It was proved that the new self-bias circuit reduced gain variation between chips from 0.8dB RMS to 0.3 dB RMS.

II. OPEARATION PRINCIPLE

The schematic diagram of the proposed bias circuit is shown in Fig.1. The principle of process variation compensation resembles that of [8]. FET1 is fabricated in the same process technology that the microwave amplifying FET (FET2) is. Positive biases are applied at terminals Vdd and Vgg for single bias operation. (It is preferable that these values are equal for simplicity of external bias circuit.) Note that FET1 works only as a part of bias circuit and does not have any microwave amplification.

Potential division between resistors from R1 to R4 and FET1 defines the gate potential of FET2 V_{g2},

$$V_{gg} = I_1(R_3 + R_4) + V_{ds}^{FET1} \quad ...(1)$$

$$I_1 = f\left(-I_1 R_4, V_{ds}^{FET1}\right) \quad ...(2)$$

$$V_{g2} = \frac{R_2}{R_1 + R_2}\left(V_{gg} - R_3 I_1\right) \quad ...(3)$$

where $f(V_{gs}, V_{ds})$ describes the Id-Vd characteristic of FET1 (and FET2 also) and R1,R2 >> R3, R4. The drain current that go through FET2 (microwave amplifying FET) is determined by V_{g2} and Rs ;

$$I_2 = f\left(V_{g2} - R_s, V_{ds}^{FET2}\right) \quad ...(4)$$

$$V_{dd} = V_{ds}^{FET2} + I_2(R_s + R_d) \quad ...(5)$$

where Rd is added to suppress low frequency oscillation caused by drain bias loop of multi-stage amplifier.

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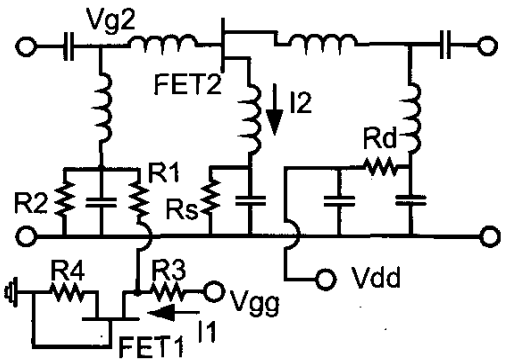


Fig. 1. Schematic diagram of self-bias amplifier with bias circuit for process variation compensation.

The operation principle of the bias circuit shown in Fig.1 as a process variation compensation circuit is as follows;

1) Assuming that the gate bias voltage that is required to set a given drain current of FET2 (say 5mA for Wg=80um) slightly shifts to a larger value due to the process variation within a wafer or within a lot. The drain current would decrease for the case of usual self-bias.

2) The current that goes through FET1 (I_1) also decreases because FET1 and FET2 are formed closely within a small chip with all the same fabrication process.

3) As the gate voltage for FET2, V_{g2} is given by (1)-(3), the decrease of I_1 increase V_{g2} and the drain current of FET2 (I_2) will partially recovered and gain variation due to process variation will be also partially compensated.

The process variation compensation effect of the proposed bias circuit was calculated by self-consistently solving equations (1)-(5) on the assumptions shown below.

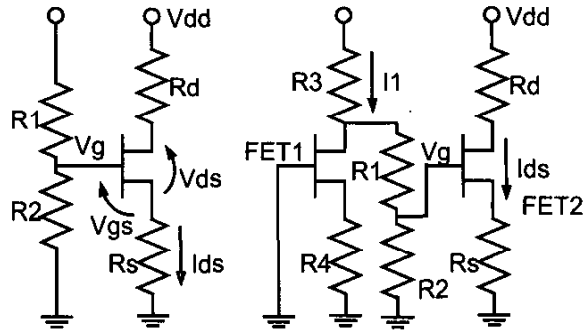
1) Process variations cause parallel shifts in Id-Vg characteristics of FETs. It means that if pinch off voltage shifts some amount ΔVp, the gate to source voltage to set a given drain current (say 5mA for Wg=80um) also shifts from Vg to Vg+ΔVp.

2) The changes of process parameters of FETs are similar in a single chip.

We have calculated the changes of drain currents due to process variation of ΔVp of from –300mV to 300mV on the above assumptions for three cases shown in Fig. 2.

By increasing Rs from 32Ω to 92Ω and increasing V_{g2} to maintain nominal drain current (=b), the variation of drain currents caused by process variation is suppressed to half of the case of usual self-bias (=a). This is caused by increase of self-compensation effect by feedback resistor Rs. When the proposed bias circuit is employed (=c), the drain current variation is even reduced to 1/3 of usual self-bias case. (shown in Fig. 3)

In general, variations of gains of amplifiers are mostly caused by variations of drain currents and trans-conductances. Therefore, suppressing variation of drain currents is very effective to suppress gain variations, which is pretty desirable to amplifiers for use in APAA modules.



(a) Usual self-bias (Vg=0) (c) Proposed bias circuit
(b) Rs increased (Vg=+0.3V)

Fig. 2. DC equivalent circuits of proposed bias circuit and usual self-bias circuit for calculation of drain current change due to process variation.

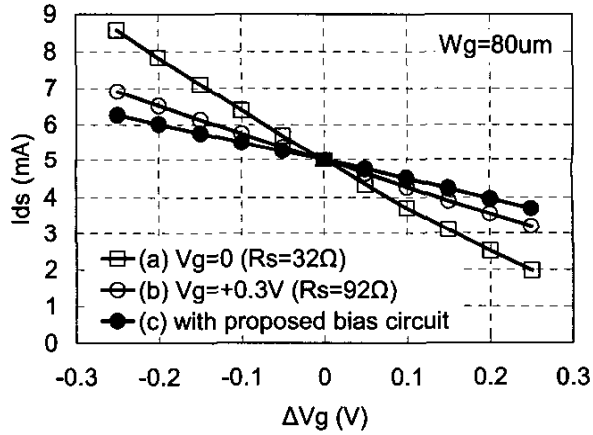


Fig. 3. Calculated drain current variation due to process variation of ΔVp of from –300mV to 300mV.

III. Experimental

The proposed bias circuit has been implemented in a Ka-band three stage self-bias GaAs low noise MMIC amplifier. The photograph of the chip is shown in Fig. 4. It employs three AlGaAs/InGaAs pHEMTs for low noise operation in Ka-band, whose gate length and gate width are 0.25μm and 80μm respectively, loaded with source inductors for simultaneous noise and gain matching and

self-bias feedback resistors with RF shunt capacitors. To achieve small chip size, high impedance microstrip lines (W=10μm) are used for matching elements. The proposed bias circuit is comprised of one 80x2μm FET (all the same as microwave amplifying FETs) and three resistors. The total chip size is as small as 1.62x1.22mm^2 and chip area shared for the bias circuit is less than 5% of it. In Fig. 4, R1 is split into four resistors to prevent unexpected gate bias loop oscillation.

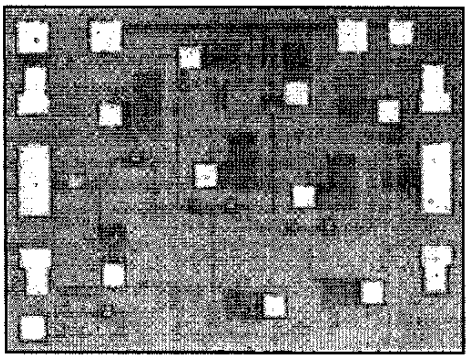


Fig. 4. Picture of Ka-band self-bias low noise GaAs MMIC amplifier with bias circuit for process variation compensation. The chip dimension is 1.62mm x 1.22mm.

The S-parameters and noise figures of manufactured chips were evaluated on-wafer at room temperature. The external bias voltage Vgg was kept at a constant value of 5.0 V. Fig. 5 shows the typical measured S-parameters and noise figures of the amplifiers. The amplifiers showed a gain of > 20dB, a noise figure of < 1.8dB, input and output return losses of > 10dB at 29GHz.

Distribution of gains at 29 GHz against drain current is shown in Fig 6 for with and without proposed bias circuit. As we expected, distribution of drain current is drastically reduced from 2.2 mA RMS to 1.1 mA RMS. The gain distribution at 29GHz was refined from 0.8dB RMS to 0.3 dB RMS by employing the new bias circuit.

As for the low noise amplifiers that work in high frequency regime of microwave (i.e. quasi-millimeter wave) such as this work, variations of gain directly reflect to variations of noise figures. This is because gain of the 1st stage is not enough to eliminate the noise contribution of 2nd stage and later. (Gain of the 1st stage is 7~8dB as for this work) In fact, variation of noise figure was also reduced from 1.8dB +/- 0.3dB to +/- 0.05dB by employing proposed bias circuit. Considering mass production, this fact is very important because yield of low noise amplifiers are mainly limited by both gain and noise figure characteristics. These measurement results suggest that yield of self-bias low noise MMIC amplifiers will be raised by applying proposed technique through reduction of variation in gain together with in noise figure.

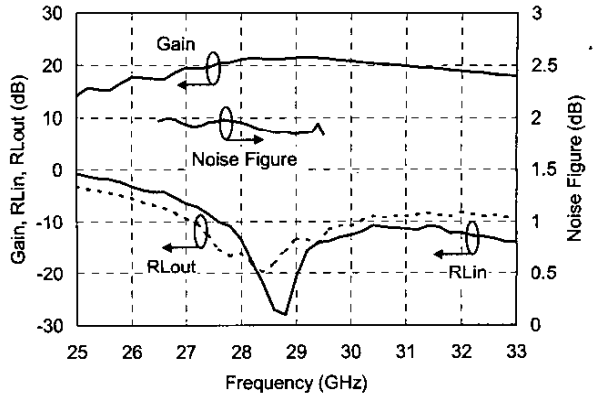


Fig. 5. Typical S-parameters and noise figure of Ka-band three-stage self-bias low noise amplifier equipped with proposed bias circuit. Measured with Vdd=3.0V, Vgg=5.0V at room temperature.

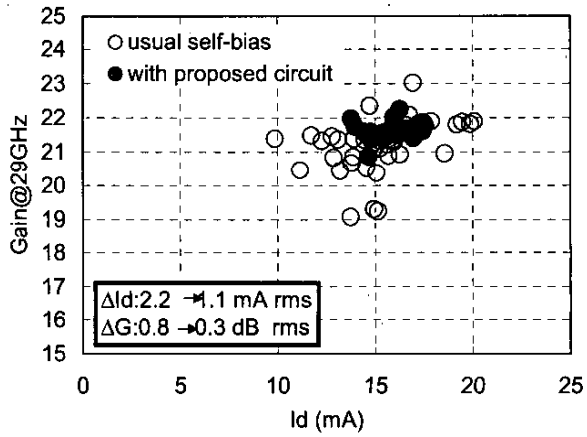


Fig. 6. Distribution of gains at 29 GHz against drain currents for with (indicated by filled circle) and without (indicated by open circle) proposed bias circuit.

IV. Conclusion

In conclusion, we have developed a new self-bias circuit embedded in a low noise MMIC amplifier that compensates gain variation between chips due to process variations. A Ka-band low noise MMIC amplifier with proposed gate-bias circuit was designed and manufactured. The proposed bias circuit reduced gain variation between chips from 0.8dB to 0.3dB in RMS. The chip area consumed for the bias circuit was less than 5% of the total chip size of 1.98mm^2. We conceive that this bias circuit will contribute to high yield of self-bias MMIC amplifiers and drastically reduce the total cost of active phased array antennas.

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